WHAT IS CLAIMED IS:

1. A method for manufacturing integrated circuit devices including capacitor structures, the method comprising:

providing a substrate, including an overlying thickness of first insulating material;

forming a plurality of openings within the thickness of the first insulating material and a region of the dielectric material, each of the openings including a width and a height;

forming a barrier layer overlying an exposed surface of each of the plurality of openings;

filling each of the openings with a metal layer, the metal layer occupying substantially an entire region of each of the openings to form a plurality of metal structures, each of the metal structure having a width and height;

planarizing a surface of the metal layer;

patterning the region to expose each of the metal structures to expose the barrier layer overlying each of the metal structures;

forming an insulating layer overlying each of the exposed barrier layer structures; and

forming a second metal layer overlying the capacitor insulating layer overlying the barrier layer structures, whereupon each of the metal layer structures, overlying capacitor insulating layer, and second metal layer form a capacitor structure; and

planarizing the second metal layer.

2. The method of claim 1 wherein the metal structures comprise substantially copper material or tungsten or aluminum.

3. The method of claim 1 wherein the insulating layer is silicon nitride or PECVD silicon nitride.

4. The method of claim 1 wherein the insulating layer is maintained at a temperature below 400 degrees Celsius.

5. The method of claim 1 further comprising forming a dual damascene interconnect structure within the first insulating material concurrently with one or more of the steps of forming the integrated circuit.

6. The method of claim 1 wherein the barrier metal layer comprises tantalum nitride.

7. The method of claim 1 wherein the second metal layer comprises tungsten, the tungsten filing the region occupied by the plurality of metal structures.

8. The method of claim 1 wherein the patterning comprises selective removal of a portion of the first insulating material to expose the plurality of metal structures.

9. The method of claim 8 wherein the selective removal uses an etchant selected from C_4F_8, CO, O_2, CF_4N_2, $ArSF_6$, CHF_3. CH_3F. C_4F_6. and C_2F_6.

10. The method of claim 1 wherein the integrated circuit is a mixed mode signal device.

11. A semiconductor integrated circuit device structure comprising:

a substrate;

a thickness of first insulating material overlying the substrate;

a capacitor region within the thickness of the first insulating material, the capacitor region extending from a lower surface of the first insulating material to an upper surface of the first insulating material, the capacitor region including a width, the width extending from the lower surface to the upper surface;

a contact region overlying the substrate within at least the capacitor region;

a lower capacitor plate formed from a plurality of vertical metal structures defined within the capacitor region and connected to the contact region, each of the plurality of vertical metal structures including a width and a height, each of the plurality of vertical metal structures being substantially parallel to each other along a length of the height of each of the vertical metal structures;

a barrier metal layer formed overlying exposed surfaces of each of the plurality of vertical metal structures;

a capacitor dielectric layer overlying each of the exposed surfaces of the barrier layer on each of the vertical metal structures; and

an upper capacitor plate formed from metal material within the capacitor region overlying surfaces of the capacitor dielectric layer; and

a planarized surface formed from the upper capacitor plate.

12. The device of claim 11 wherein the metal material fills the capacitor region defined in the thickness of first insulating material.

13. The device of claim 11 wherein the capacitor dielectric layer comprises an oxide.

14. The device of claim 12 wherein the lower capacitor plate comprises a copper material.

15. The device of claim 11 wherein the lower capacitor plate, the capacitor dielectric, and upper capacitor plate define a metal insulator metal capacitor for a mixed signal device.

16. The device of claim 11 further comprising an interconnect region defined within the thickness of first insulating material, the interconnect region being outside of the capacitor region.

17. A method for manufacturing integrated circuit devices including capacitor structures, the method comprising:

providing a semiconductor substrate;

forming an overlying thickness of first insulating material on the semiconductor substrate;

defining a capacitor region and an interconnect region;

forming a plurality of openings within the thickness of the first insulating material and the capacitor region of the first insulating material, each of the openings including a width and a height;

forming a plurality of openings within the thickness of first insulating material in the interconnect region;

forming a barrier layer overlying an exposed surface of each of the plurality of openings in the capacitor region and the interconnect region;

filling each of the openings with a metal material, the metal material occupying substantially an entire region of each of the openings to form a plurality of metal structures, each of the metal structure having a width and height;

planarizing a surface region of each of the metal structures;

patterning the capacitor region to expose the barrier layer on each of the metal structures to form an opening within the capacitor region excluding the plurality of metal structures and barrier layer, the plurality of metal structures and barrier layer forming a first electrode structure of a capacitor;

forming an insulating layer overlying each of the exposed barrier layer structures to form a capacitor dielectric for the capacitor;

filling the opening within the capacitor region using a second metal layer overlying the capacitor insulating layer to form a second electrode structure of the capacitor; and

planarizing the second metal layer.

18. The method of claim 17 wherein the second metal layer comprises a copper material.

19. The method of claim 17 wherein the metal material is copper fill material.